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MICROELECTRONICS

Theory, Design, and Fabrication

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CHAPTER 5

SEMICONDUCTOR INTEGRATED CIRCUITS

By Gordon E. Moore

5-1. INTRODUCTION

If miniaturization were the sole justification for microelectronics, an improvement of the order of a factor of 10^3 in volumetric efficiency could be achieved merely by elimination of the packing voids in conventional electronics. The cost of this type of assembly can be easily justified (see Chap. 3) for special applications where volume and weight are at a premium. The excitement created by microelectronics, however, extends far beyond size and weight alone. The potential achievements in the reduction of cost and in the improvement of reliability point the way to an entirely new realm of allowable system complexity. The actual achievements to date, though considerably more modest than the publicity might lead one to believe, suggest that microelectronics will be employed extensively from now on. An important approach to this exciting field is provided by semiconductor integrated circuitry. This should not be viewed as a completely independent entity from other approaches, for example, thin films, but rather as a complementary approach evolving toward the same general goal but arising from a different technological background. The origin of this evolutionary process sprang naturally from the transistor and diode technology. It is being extended to include more and more complex combinations of operations.

Before we proceed further, some definition of semiconductor integrated circuitry is required, because this term or similar terms have been applied to a wide variety of levels of sophistication. There are two extremes in semiconductor integrated circuitry. The first of these is the *chip approach* wherein individual components, such as transistors, resistors, and diodes, are produced on separate pieces of material; then these separate components are mounted and interconnected in a single package to produce a circuit function by what is, in reality, a microassembly technique.

The second extreme makes the entire electronic function in and upon a single piece of semiconductor material having many components or regions that are isolated or interconnected electrically, as the circuit requires. In general, in this latter approach, all the intraconnections within the functional block itself will be done by batch processing on large numbers of circuits. The only individual assembly operations are associated with mounting the final circuit function in a package, so that it can be connected conveniently to the outside world.

All levels between these two extremes are practiced. The level of integration will, in general, be determined at any time by the degree of development of the technology and such economic considerations as the number of identical circuits needed and the time scale.

The approach employing individual components offers the advantage of complete flexibility, analogous to that obtainable in conventional electronics. Individual chips are interconnected by lead-bonding techniques essentially identical with those employed in transistor manufacture. A circuit made from individual chips mounted on a metallized ceramic substrate is shown in Fig. 5-1. More elaborate schemes wherein the individual components are mounted in precise locations on a substrate and where the separations between individual components are filled with a material suitable for thin-film interconnections have been proposed. None of these schemes have been developed adequately enough so that they can be seriously considered at the present.

This chapter will be concerned primarily with the other extreme of semiconductor integrated circuits—those which are produced entirely

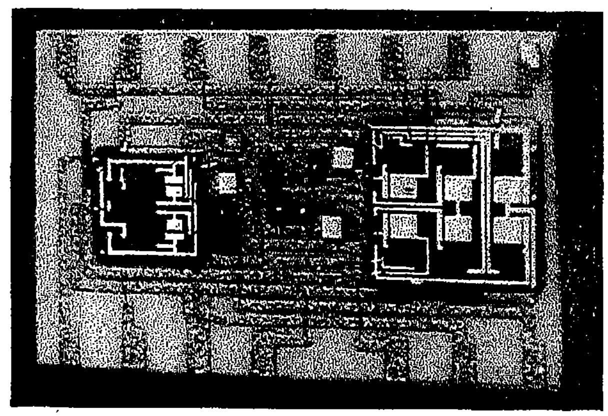

FIG. 5-1. A hybrid integrated circuit made from separate diode and transistor chips and resistor arrays, mounted upon a metallized ceramic substrate. The size of the ceramic substrate is 0.325 by 0.575 in. (*General Instrument Corporation.*)

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in a single monolithic block of material. Examples are solid circuits produced by Texas Instruments, Inc., and micrologic circuits produced by Fairchild Camera and Instrument Corporation. Intermediate cases can usually be considered as the single-chip approach applied to smaller monolithic blocks: for example, the molecular electronics used by Westinghouse in the AN/ARC-63 transceiver.[1] The only semiconductor materials which need be considered for their applicability to integrated circuits, at present, are germanium and silicon. Since the trend toward integrated circuits arose after the silicon technology was well developed, and indeed was, to a considerable extent, stimulated by this technology, germanium has not been an important material. Accordingly the discussion will be restricted to silicon. It is unlikely that other semiconductor materials, such as, for example, gallium arsenide, will be of importance in the field of integrated circuitry for other than a few highly specialized applications.

The large-scale manufacture of silicon mesa transistors by batch processing had been accomplished before the rise of semiconductor integrated circuits. Such mesa transistors are made in an array covering a slice of silicon material of the order of one inch in diameter. Typical arrays of double-diffused silicon transistors are shown in Fig. 5-2. Such a wafer may contain as many as 1,000 transistor structures. These mesa transistors are completed electrically while still in wafer form. They are positioned in a precise geometric array. The manufacturing operation beyond this stage consists of separating these structures, mounting them, and selling them to a customer, who proceeds to reconnect them to form circuits. Since this dicing and assembly is the major expense in making small transistors, one is led rather naturally to consider per-

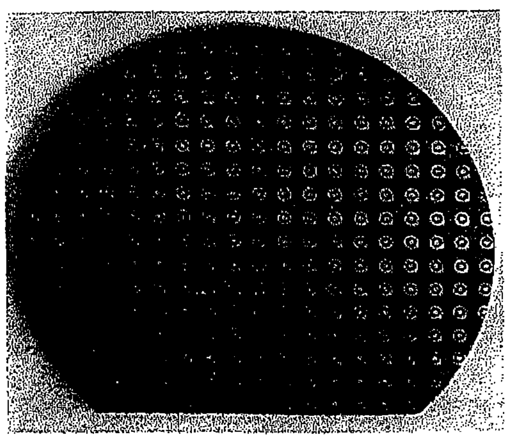

FIG. 5-2. A typical array of double-diffused silicon transistors. Each ring-and-dot pattern is a transistor structure. Only the metallized emitter and base contacts are visible in this photomicrograph. The silicon wafer is approximately one inch in diameter. The flat edge is used for indexing during process.

forming interconnections between the structures without loss of index, in order to decrease total system-manufacturing costs.

Several problems arise when this is considered. First, the surfaces of mesa transistors are extremely sensitive to ambient, resulting in relatively low yields from devices at the wafer stage to good final products. This problem is aggravated by increasing the number of devices or by attempting to run interconnections over the surfaces. Interconnections by bonding of leads can be accomplished successfully. However, this is a unit-by-unit operation, and reinserts the expensive portion of semiconductor-device manufacture while decreasing yields because of the increased number of possibilities for imperfections as the complexity of the interconnected unit increases.

The next important step in making semiconductor integrated circuitry practical was achieved with the development of the planar transistor structure.[2] The schematic cross sections of a single planar transistor structure and a mesa transistor are shown in Fig. 5-3. The advantages of the planar structure are intimately tied to the silicon dioxide layer covering the region where the junctions intersect the surface. The oxide layer is an effective barrier to the deleterious effects of the ambient on the junction surfaces. In addition, it supplies a relatively flat surface, upon which thin metal intraconnections can be applied. Although this oxide layer is actually a micron or less in thickness, it has a dielectric strength ranging to several hundred volts, allowing metal films to pass over the junction regions without effect. Thus, in the planar structure, the interconnection problem for the individual components is solved. In order to make complete circuits, it is necessary to add the capability of making other elements, such as resistors and capacitors, as well as to achieve the required electrical isolation of these components. This chapter will discuss the technology and device structures available for the

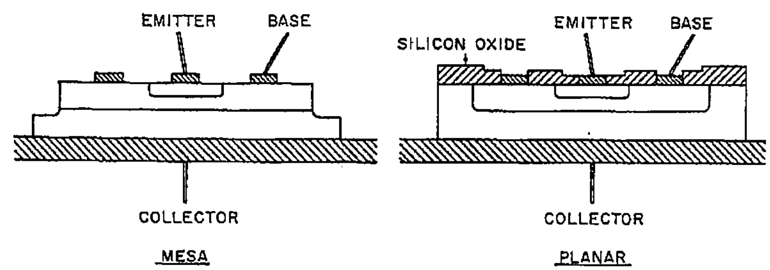

FIG. 5-3. Schematic cross sections of mesa and planar transistors. The metal emitter, base, and collector contacts normally employed are shown. Note the silicon oxide layer covering the intersection of the junctions with the surface in the planar case.